REMARKS

Claims 1-7 and 9-14 are pending in the present application. Claims 1, 3, 4 and 10-14 have been amended. Claim 8 has been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Information Disclosure Statement

An Information Disclosure Statement has been filed concurrently herewith. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the documents as submitted therewith have been considered and will be cited of record in the present application**.

Disclosure

Responsive to the Examiner's request, the title of the invention has been amended as "CLOCK CONTROL CIRCUIT AND CLOCK CONTROL METHOD THAT SWITCHINGLY SUPPLIES A HIGH-SPEED CLOCK AND A LOW-SPEED CLOCK", to be more clearly indicative of the invention. The Examiner is respectfully requested to approve the amended title, or in the alternative to suggest a more appropriate title.

Claim Rejections-35 U.S.C. 112

Claim 8 has been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Claim 8 has been canceled merely to advance prosecution of this application. The Examiner is therefore respectfully requested to withdraw this rejection.

Claim Rejections-35 U.S.C. 103

Claims 1, 2, 5-12 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Swoboda et al. reference (U.S. Patent No. 5,903,746) in view of Applicant's admitted prior art (AAPA). This rejection is respectfully traversed for the following reasons.

The Examiner has asserted that the Swoboda et al. reference discloses all the features of claim 1, except for explicitly disclosing that when an interrupt signal is supplied, counting of a low-speed clock is started, and when a count value reaches a value set in a register, a second control section outputs a selection signal for causing a high-speed clock to be selected. In an effort to overcome this acknowledged deficiency of the Swoboda et al. reference, the Examiner has relied upon Applicant's admitted prior art on pages 2 and 3, in the manner noted on page 4 of the current Office Action dated July 6, 2006. The Examiner has alleged that it would have been obvious to combine the teaching of the Swoboda et al. reference in Applicant's admitted prior art "because they are both directed to a clock control system", and because the teaching of

Applicant's admitted prior art would allegedly improve the performance and reliability of the system of the Swoboda et al. reference. Applicant respectfully disagrees for the following reasons.

As described beginning on page 1 of the Background of the Invention section of the present application, Applicant's admitted prior art reduces consumption of electric power by **stopping an operation clock** which is supplied to a central processing unit (CPU). As further described on page 2, at such a portable terminal, when processing by the CPU is completed, a control signal **for stopping** the oscillation circuit is output from the CPU. In this way, the high-speed operation clock generated by the oscillation circuit is stopped. During this time when provision of the high-speed clock signal to the CPU is stopped, the low frequency clock is counted, and when the count value of the low-speed clock reaches a given value, operation of the oscillation circuit is resumed and the high speed clock signal is output to the CPU. As summarized on page 3 of the present application, in the described conventional system, when processing of the CPU is completed, the clock signal for the CPU **is completely stopped**.

Accordingly, in Applicant's admitted prior art, the high-speed operation clock provided from the oscillator to the CPU is stopped during a standby mode, so that no clock signal is provided to the CPU. In contrast, claim 1 features in combination a second control section which "when the standby mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected". That is, the low-speed clock is provided to the central processing unit during the

standby mode. Applicant's admitted prior art as relied upon by the Examiner does not disclose these features. Applicant's admitted prior art as specifically relied upon thus cannot provide the necessary motivation to modify the system of the Swoboda et al. reference to provide a low-speed clock to a CPU during a standby mode, and to count the low-speed clock when an interrupt signal is received as the low-speed clock is provided to the CPU, so that when a count value of the low-speed clock reaches a set value, the high-speed clock is selected to be provided to the CPU instead of the low-speed clock. Applicant therefore respectfully submits that the clock control circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1, 4-7 and 9-12 is improper for at least these reasons.

The clock control method of claim 14 features in combination selecting and outputting the low-speed clock as the clock signal to the central processing unit during the standby mode, and counting the low-speed clock when an interrupt signal is supplied, so that when the count value reaches a set value, the high-speed clock is selected and output as the clock signal to the central processing unit.

Applicant respectfully submits that Applicant's admitted prior art as specifically relied upon by the Examiner would provide no motivation to modify the system of the Swoboda et al. reference as would be necessary to meet the features of claim 14. Applicant therefore respectfully submits that the clock control method of claim 14 would not have been obvious in view of the prior art as relied upon by the Examiner taken

singularly or together, and that this rejection of claim 14 is therefore improper.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 3, 4 and 13 have been rejected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant however respectfully submits that claims 3, 4 and 13 should be allowable by virtue of dependency upon claim 1 for the reasons as set forth above, and that if further amendment of these claims to be in independent form is therefore unnecessary.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

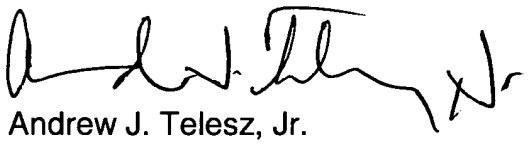
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to January 6, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $1020.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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